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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/731,453	JOSHI ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 47-54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 now recites a substrate **not** containing a chip pad, and a RDL **on** the chip pad.

It is unclear how the RDL can be attached to the chip pad if the chip pad isn't present on the substrate. As a result, it is impossible to understand the claim, let alone reject the claim over prior art. Clarification and/or correction is required.

Response to Arguments

Applicant's arguments filed 5/13/09 have been fully considered but they are not persuasive. Eight arguments have been presented with respect to the rejection of the claims.

First, it is argued that a stud bump is different from a solder bump and therefore can't be an equivalent to a solder bump.

Please note that the reject relies upon the equivalence of a solder bump and a stud bump in that they are both very well known and used methods of electrically

attaching substrates. The equivalence is in this commonality, which is their known use as an attachment method.

The second argument is that AAPA teaches a Si substrate so why would one be motivated to substitute the Si substrate for a leadframe.

Please note that the while AAPA does teach a Si substrate, it is Shibata that teaches the leadframe substrate to which the Si substrate is attached, as noted in the claims. The package of AAPA must be attached to something to make it useful. Shibata teaches attaching a chip to a leadframe. It appears that the rejection was misunderstood because the leadframe is not being substituted for the Si substrate, it is being attached to the Si substrate, as in the claims.

The next argument is that rejection of the conductive particles comprising a metal with an insulating layer and therefore the operation of AAPA and Shibata would be changed because Shibata requires alloy bonding.

Please note that Shibata is relied upon to teach the fact that it is known to attach the package of AAPA to a leadframe. Therefore, it is a secondary reference modifying the primary reference. Kaneda is relied upon to teach using conductive particles comprising a metal with an insulating layer and also modifies the primary reference (AAPA). So it is not Shibata that is being modified, it is AAPA that is being modified by Kaneda.

The fourth argument is that AAPA teaches using a polymeric material and not a polymeric material.

As noted in the rejection, insulating layers are commonly known to be made of both polymeric and non-polymeric materials. The use of one over the other is obvious because they are both commonly known and used and are conventional materials used to perform their known function.

Further, it is argued that that one would not be motivated to modify the art to arrive at a Pd coated Cu wire because Shibata already teaches a gold plating on the pads.

Please note that the combination would completely substitute the prior art bumps with Pd coated bumps. Therefore, the question as to why one would further add a Pd coating to a Cu plating is irrelevant. The use of Pd coated bumps is more than well known in the art to each and every skilled artisan.

Also, it is argued that the new limitation of claim 72 requiring the substrate to be made of a high glass transition material.

Please note that the use of a high glass transition material as the substrate is commonly known and used in the art to each and every skilled artisan. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

The seventh argument is that it is would not have been obvious to remove the UBM of AAPA because it is “desired”, as required by MPEP 2144.04(II).

Please note that this argument has been addressed in previous office actions and is restated here. Clearly, the main point is that it is obvious to omit an element and its function in situations where it isn’t “desired” for the element to be present. That is what is being stated in the rejection, that the UBM and its function are removed.

Situations where the element isn't "desired" are situations where cost is a concern. By eliminating the UBM, the cost is reduced.

The final argument is that the new limitation of claim 47 wherein the substrate does NOT contain a chip pad is not taught in the cited prior art.

Please note, as recited above, that it is unclear how the substrate can not have a chip pad but the RDL is attached to the chip pad in the next limitation. Clarification and/or correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 47-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereafter AAPA) Figures 1-3, in view of Shibata, US Patent 6,461,890 and Kaneda et al., US Patent 6,223,429.

AAPA teaches a wafer-level chip scale package, comprising:

a substrate [5] containing a chip pad [40];

a re-distributed line (RDL) pattern [20] on the chip pad;

an insulating layer [25] covering a portion of the RDL pattern;

a stud bump [35] located on the portion of the RDL pattern not covered by the insulating layer.

AAPA fails to teach a leadframe substrate containing a bond pad; and

an adhesive material containing conductive particles located between the chip and the substrate.

Shibata (Figures 5 & 6) teaches:

a chip [10] containing a stud bump [11];

a leadframe substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the leadframe with the claimed conductive adhesive because it is conventionally known in the art to connect a chip to a leadframe using a conductive adhesive. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Further, AAPA and Shibata fail to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Lastly, AAPA, Shibata and Kaneda fail to teach the insulating layer comprises a non-polymeric dielectric material.

AAPA is silent as to the specific material used as the insulating layer that covers the RDL, the use of a non-polymeric insulator would have been obvious to one of ordinary skill in the art because insulating layers are known to be made of both polymeric and non-polymeric materials, such as silicon dioxide, are commonly known generic materials used as insulating layers. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Regarding claim 48, Shibata teaches at least one conductive particle is located between the stud bump and the bond pad (figure 6).

With respect to claim 49, Shibata teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

As to claim 50, Shibata, which teaches the bump is made of gold (7, 45+), teaches the package does not contain any solder paste.

In re claim 51, while Shibata, which teaches the use of gold (Au) bumps (7, 45+), fails to teach the stud bump comprises Cu, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Cu in the invention of Shibata because Au and Cu are materials known to a skilled artisan to be equivalent. Both are well known in the art materials used as bumps, as taught by Tummala et al., Microelectronics Packaging Handbook: Semiconductor Packaging - Part II, 1997, pp II-207. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Regarding claim 52, AAPA, Shibata and Kaneda fail to teach the stud bump is formed by wire bonding a Pd coated copper wire to the RDL pattern using a capillary to provide the stud bump with a coined shape.

Please note that using by wire bonding a Pd coated copper wire to the RDL pattern using a capillary to provide the stud bump is a process limitation is a product claim and therefore isn't given any patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product

was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)

Further, relating to the coined shape, while Shibata fails to teach the stud bump is a coined stud bump, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a coined stud bump in the invention of Shibata because the use of a stud bump or a coined stud bump are equivalent. A skilled artisan knows that each are commonly known and used bumps to interconnect a die to a substrate, as taught by Lau, Flip Chip Technologies, 1996, pp. 129-131. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Lastly, while AAPA and Shibata fail to teach the use a Pd coated bump or a bump that includes Pd (the bump resulting form a Pd-coated Cu wire would either be coated by or include/alloy with Pd upon reflow), it would have been obvious to one of ordinary skill in the art at the time of the invention to use Pd and Cu bumps in the invention of AAPA and Shibata because they are conventionally known and used in the art. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

With respect to claim 53, while AAPA fails to teach the insulating layer comprises silicon nitride, silicon oxide, or silicon oxynitride, it would have been obvious to one of

ordinary skill in the art at the time of the invention to use silicon nitride, silicon oxide, or silicon oxynitride as the insulating layer in the invention of AAPA because they are conventionally known and used insulating layers known to each and every skilled artisan. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

As to claim 54, while AAPA fails to teach there is no under bump metal under the stud bump, it would have been obvious to one of ordinary skill in the art at the time of the invention to remove the UBM of AAPA because the omission of an element and its function is obvious if the function of the element is not desired (MPEP 2144.04 IIA). The device would work without the UBM, therefore it would be obvious to remove it and its desired function in order to reduce cost.

Claims 55-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereafter AAPA) Figures 1-3, in view of Shibata, US Patent 6,461,890 and Kaneda et al., US Patent 6,223,429.

AAPA teaches a wafer-level chip scale package, comprising:

a substrate [5] containing a chip pad [40];

a re-distributed line (RDL) pattern [20] on the chip pad;

an insulating layer [25] covering a portion of the RDL pattern;

a stud bump [35] located on the portion of the RDL pattern not covered by the insulating layer.

AAPA fails to teach a leadframe substrate containing a bond pad; and

an adhesive material containing conductive particles located between the chip and the substrate.

Shibata (Figures 5 & 6) teaches:

a chip [10] containing a stud bump [11];

a leadframe substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the leadframe with the claimed conductive adhesive because it is conventionally known in the art to connect a chip to a leadframe using a conductive adhesive. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Further, AAPA and Shibata fail to teach the conductive particles comprise metal with an insulating layer with an insulating layer with at least one conductive particle contacting both the stud bump and the bond pad.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer with at least one conductive particle contacting both the stud bump and the bond pad.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Also, AAPA, Shibata and Kaneda fail to teach the insulating layer comprises a non-polymeric dielectric material.

AAPA is silent as to the specific material used as the insulating layer that covers the RDL, the use of a non-polymeric insulator would have been obvious to one of ordinary skill in the art because insulating layers are known to be made of both polymeric and non-polymeric materials, such as silicon dioxide, are commonly known generic materials used as insulating layers. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Lastly, AAPA fails to teach the stud bump contains Cu.

While Shibata, which teaches the use of gold (Au) bumps (7, 45+), fails to teach the stud bump comprises Cu, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Cu in the invention of Shibata because Au and Cu are materials known to a skilled artisan to be equivalent. Both are well known in the art materials used as bumps, as taught by Tummala et al., Microelectronics Packaging Handbook: Semiconductor Packaging - Part II, 1997, pp II- 207. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

With respect to claim 56, Shibata teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

As to claim 57, Shibata, which teaches the bump is made of gold (7, 45+), teaches the package does not contain any solder paste.

With respect to claim 58, while AAPA fails to teach the insulating layer comprises silicon nitride, silicon oxide, or silicon oxynitride, it would have been obvious to one of ordinary skill in the art at the time of the invention to use silicon nitride, silicon oxide, or silicon oxynitride as the insulating layer in the invention of AAPA because they are conventionally known and used insulating layers known to each and every skilled artisan. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

As to claim 59, while AAPA fails to teach there is no under bump metal under the stud bump, it would have been obvious to one of ordinary skill in the art at the time of the invention to remove the UBM of AAPA because the omission of an element and its function is obvious if the function of the element is not desired (MPEP 2144.04 IIA). The device would work without the UBM, therefore it would be obvious to remove it and its desired function in order to reduce cost.

Regarding claim 60, AAPA, Shibata and Kaneda fail to teach the stud bump is formed by wire bonding a Pd coated copper wire to the RDL pattern using a capillary to provide the stud bump with a coined shape.

Please note that using by wire bonding a Pd coated copper wire to the RDL pattern using a capillary to provide the stud bump is a process limitation is a product claim and therefore isn't given any patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)

Further, relating to the coined shape, while Shibata fails to teach the stud bump is a coined stud bump, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a coined stud bump in the invention of Shibata because the use of a stud bump or a coined stud bump are equivalent. A skilled artisan knows that each are commonly known and used bumps to interconnect a die to a substrate, as taught by Lau, Flip Chip Technologies, 1996, pp. 129-131. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Lastly, while AAPA and Shibata fail to teach the use a Pd coated bump or a bump that includes Pd (the bump resulting form a Pd-coated Cu wire would either be

coated by or include/alloy with Pd upon reflow), it would have been obvious to one of ordinary skill in the art at the time of the invention to use Pd and Cu bumps in the invention of AAPA and Shibata because they are conventionally known and used in the art. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Claims 61, and 63-66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereafter AAPA) Figures 1-3, in view of Shibata, US Patent 6,461,890.

AAPA teaches a wafer-level chip scale package, comprising:

a substrate [5] containing an integrated circuit [40];

a re-distributed line (RDL) pattern [20] on the substrate and the integrated circuit;

an insulating layer [25] covering a portion of the RDL pattern;

a non-reflowed stud bump [35] located on the portion of the RDL pattern not covered by the insulating layer.

AAPA fails to teach a leadframe substrate containing a bond pad; and

an adhesive material containing conductive particles located between the chip and the substrate.

Shibata (Figures 5 & 6) teaches:

a chip [10] containing a stud bump [11];

a leadframe substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the leadframe with the claimed conductive adhesive because it is conventionally known in the art to connect a chip to a leadframe using a conductive adhesive. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Lastly, AAPA, and Shibata fail to teach the insulating layer comprises a non-polymeric dielectric material.

AAPA is silent as to the specific material used as the insulating layer that covers the RDL, the use of a non-polymeric insulator would have been obvious to one of ordinary skill in the art because insulating layers are known to be made of both polymeric and non-polymeric materials, such as silicon dioxide, are commonly known generic materials used as insulating layers. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Please note that while AAPA fails to specifically teach the stud bump is non-reflowed, it would have been obvious to one of ordinary skill in the art that the bump would have non-reflowed at the time of deposition and then later reflowed. Therefore, there was a point in the process wherein the stud bump was non-reflowed. This rejection relies upon that moment in time.

Regarding claim 63, Shibata teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

As to claim 64, Shibata, which teaches the bump is made of gold (7, 45+), teaches the package does not contain any solder paste.

In re claim 65, while Shibata, which teaches the use of gold (Au) bumps (7, 45+), fails to teach the stud bump comprises Cu, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Cu in the invention of Shibata because Au and Cu are materials known to a skilled artisan to be equivalent. Both are well known in the art materials used as bumps, as taught by Tummala et al., Microelectronics Packaging Handbook: Semiconductor Packaging - Part II, 1997, pp II-207. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

As to claim 66, while AAPA fails to teach there is no under bump metal under the stud bump, it would have been obvious to one of ordinary skill in the art at the time of the invention to remove the UBM of AAPA because the omission of an element and its function is obvious if the function of the element is not desired (MPEP 2144.04 IIA). The device would work without the UBM, therefore it would be obvious to remove it and its desired function in order to reduce cost.

Claim 62 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereafter AAPA) Figures 1-3, in view of Shibata, US

Patent 6,461,890, as applied to claim 61 above, and further in view of Kaneda et al., US Patent 6,223,429.

AAPA and Shibata fail to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Claims 67-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereafter AAPA) Figures 1-3, in view of Shibata, US Patent 6,461,890 and Kaneda et al., US Patent 6,223,429.

AAPA teaches an electronic apparatus containing a packaged semiconductor device without solder paste, comprising:

a substrate [5] containing a chip pad [40];

a re-distributed line (RDL) pattern [20] on the chip pad;

an insulating layer [25] covering a portion of the RDL pattern;

a stud bump [35] located on the portion of the RDL pattern not covered by the insulating layer.

AAPA fails to teach a leadframe substrate containing a bond pad; and

an adhesive material containing conductive particles located between the chip and the substrate with at least one conductive particle contacting both the stud bump and the bond pad.

Shibata (Figures 5 & 6) teaches:

a chip [10] containing a stud bump [11];

a leadframe substrate [60] containing a bond pad [61]; and

an adhesive material [30] containing conductive particles [32] located between the chip and the substrate with at least one conductive particle contacting both the stud bump and the bond pad.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the leadframe with the claimed conductive adhesive because it is conventionally known in the art to connect a chip to a leadframe using a conductive adhesive. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Further, AAPA and Shibata fail to teach the conductive particles comprise metal with an insulating layer.

Kaneda (6, 35+) teaches the conductive particles comprise metal with an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles of Kaneda in the invention of Shibata because Kaneda teaches conductive particles comprising metal with an insulating layer improves insulating properties in the lateral direction of metal particles (6, 35+).

Also, AAPA, Shibata and Kaneda fail to teach the insulating layer comprises a non-polymeric dielectric material.

AAPA is silent as to the specific material used as the insulating layer that covers the RDL, the use of a non-polymeric insulator would have been obvious to one of ordinary skill in the art because insulating layers are known to be made of both polymeric and non-polymeric materials, such as silicon dioxide, are commonly known generic materials used as insulating layers. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Lastly, AAPA fails to teach the stud bump contains Cu.

While Shibata, which teaches the use of gold (Au) bumps (7, 45+), fails to teach the stud bump comprises Cu, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Cu in the invention of Shibata because Au and Cu are materials known to a skilled artisan to be equivalent. Both are well known in the art materials used as bumps, as taught by Tummala et al., Microelectronics Packaging Handbook: Semiconductor Packaging - Part II, 1997, pp II- 207. The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Regarding claim 68, Shibata teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (7, 64+).

As to claims 69 and 72, Shibata, which teaches the bump is made of gold (7, 45+), teaches the package does not contain any solder paste.

With respect to claim 70, while AAPA fails to teach the insulating layer comprises silicon nitride, silicon oxide, or silicon oxynitride, it would have been obvious to one of ordinary skill in the art at the time of the invention to use silicon nitride, silicon oxide, or silicon oxynitride as the insulating layer in the invention of AAPA because they are conventionally known and used insulating layers known to each and every skilled artisan. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

As to claim 71, while AAPA fails to teach there is no under bump metal under the stud bump, it would have been obvious to one of ordinary skill in the art at the time of the invention to remove the UBM of AAPA because the omission of an element and its function is obvious if the function of the element is not desired (MPEP 2144.04 IIA). The device would work without the UBM, therefore it would be obvious to remove it and its desired function in order to reduce cost.

In re claim 72, while AAPA fails to teach the use of a high glass transition material as the substrate, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a high glass transition material in the invention of Shibata because high glass transition material are conventionally known and used in

the art. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-Th 7:30 AM-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571)-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David A. Zarneke/
Primary Examiner, Art Unit 2891
7/29/09